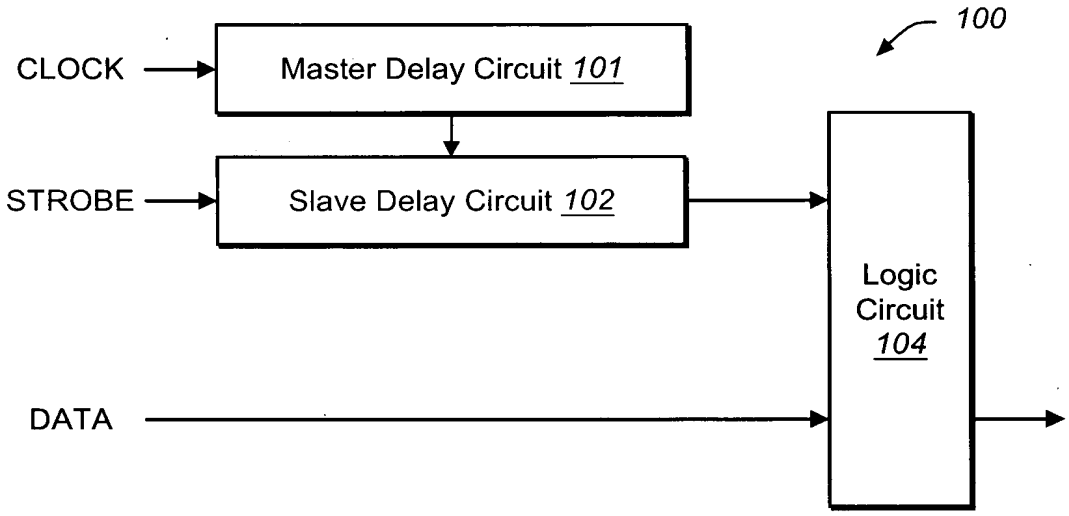

FIG._1
(PRIOR ART)

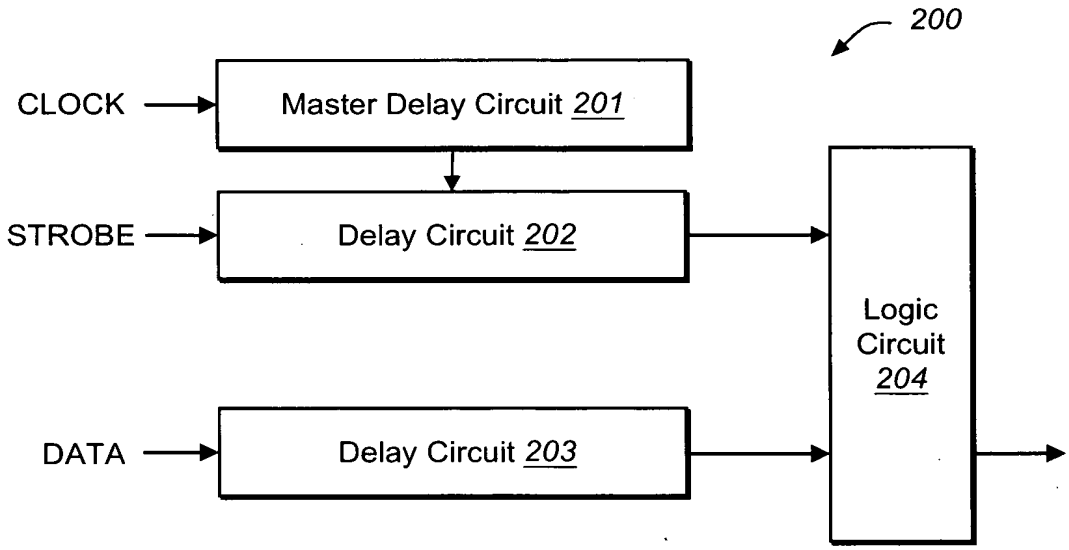

FIG._2

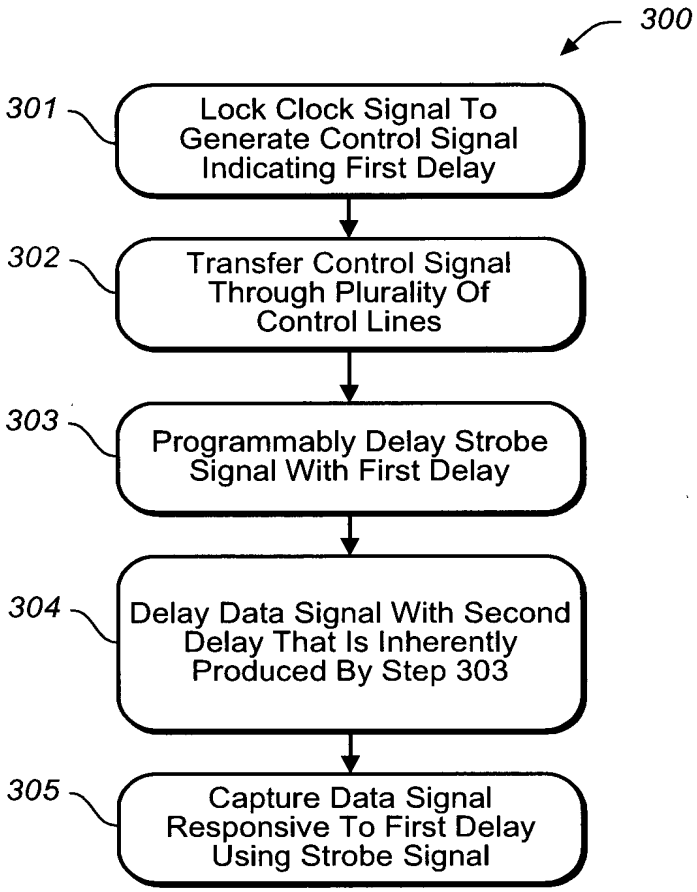
300
301
Lock Clock Signal To Generate Control Signal Indicating First Delay
302
Transfer Control Signal Through Plurality Of Control Lines
303
Programmably Delay Strobe Signal With First Delay
304
Delay Data Signal With Second Delay That Is Inherently Produced By Step 303
305
Capture Data Signal Responsive To First Delay Using Strobe Signal

FIG._3

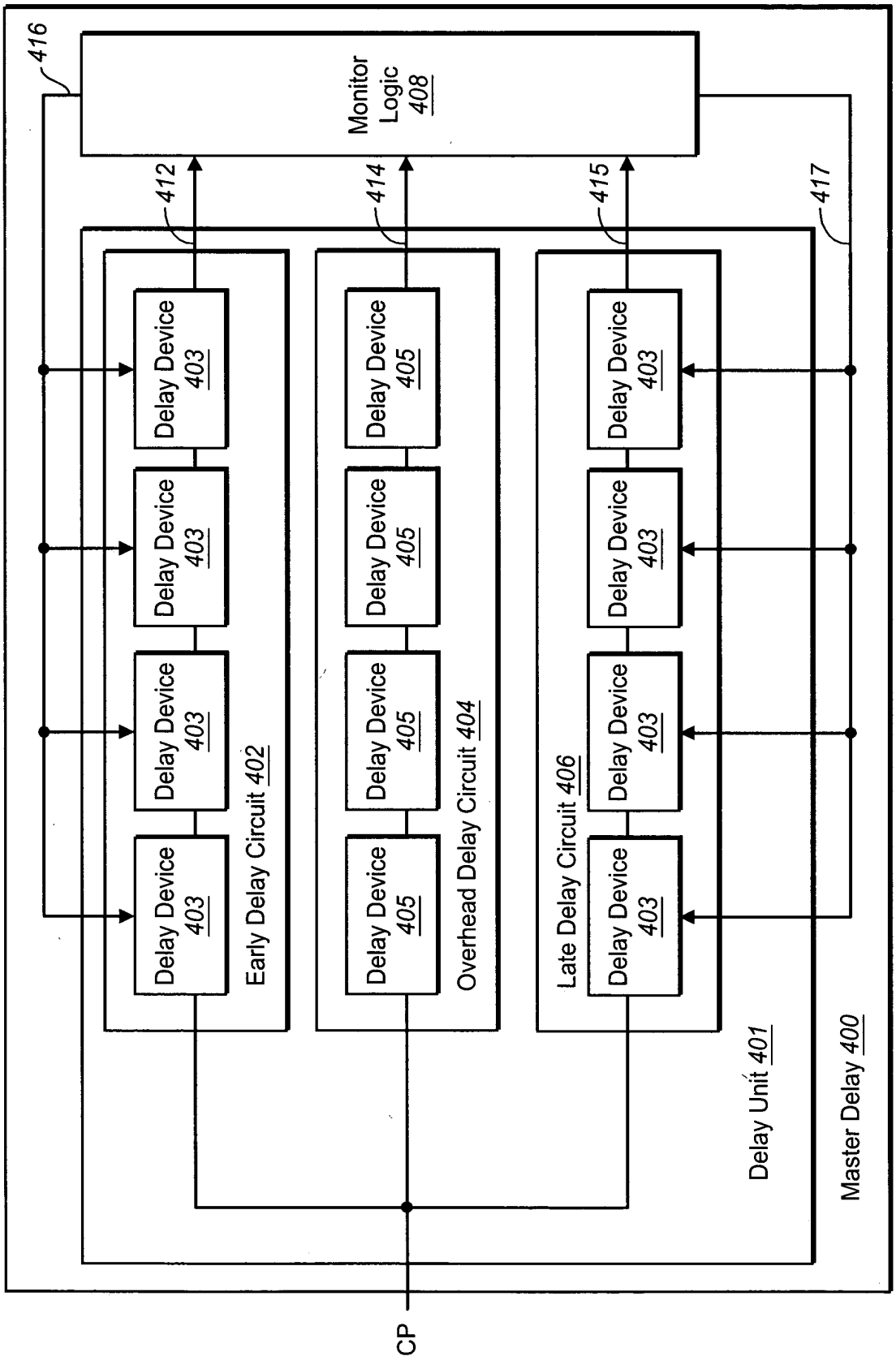
416
Monitor Logic 408
412
414
415
417
Delay Device 403
Delay Device 405
Early Delay Circuit 402
Overhead Delay Circuit 404
Late Delay Circuit 406
Delay Unit 401
Master Delay 400
CP

FIG._4